

REMARKS

Claims 1-14 are present in this application. Claims 10-14 have been added. Claims 1, 3, 5, and 8 are currently independent.

Claim 1 has been amended to incorporate the subject matter of claim 9. Claims 3, 5, and 8 have been re-written into independent claims.

New Claims

New claim 10 recites subject matter from original claim 6. New claim 11 recites subject matter from original claim 9. Claims 12-14 recite subject matter from original claim 2.

Interview

Applicant wishes to thank the Examiner for conducting the interview in the presence of Mr. Chin. Applicant believes that as a result of the interview, the Examiner now better understands the present invention, in particular with respect to the teachings of the Lee reference.

Claim Rejection – 35 USC 112

Claim 9 has been rejected under 35 U.S.C. 112, second paragraph. By this amendment, the dependency of claim 9 has been corrected.

Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 USC 102

Claims 1-8 have been rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent 6,373,913). Applicant respectfully traverses this rejection.

By this amendment, claim 1 has been amended to incorporate the subject matter of original claim 9. Claims 3, 5, and 8 have been re-written into independent form. Thus, this rejection does not apply to claim 9. In any case, Applicant submits that Lee does not teach or suggest the limitations recited in claim 1 as amended.

Based on the discussion of the Lee reference during the interview, it is Applicant's understanding that the claimed polyphase clock generation circuit and detection circuit are shown by Lee's Figure 6, as first unit delays 127 each delaying the clock signal and comparators 128, respectively. In particular, it is Applicant's understanding that the claimed detection circuit is shown by transmission gates 131 in each comparator 128.

With respect to claim 3, it is understood that the claimed logic circuit is shown by Lee's latch 132 and gate 133, and that the claimed latch circuit is shown by Lee's latch 134.

To the contrary, unlike the latch 134 of Lee, the latch circuit of claim 3 is recited as having "an output is inputted to the logic circuit." In other words, the logic circuit of the present claimed invention includes a loop/feedback circuit. Such a circuit is not shown in Lee. Thus, Applicant submits that Lee fails to teach or suggest at least the claimed "latch circuit to which an output from the logic circuit is inputted and of which an output is inputted to the logic circuit."

With respect to claim 5, Applicant submits that Lee fails to teach or suggest at least the claimed "operational circuit for sampling an output from the detection circuit a plurality of times and carrying out operations on sampled values."

With respect to claim 8, Applicant submits that Lee fails to teach or suggest at least the claimed "a plurality of bit synchronous working circuits to which a polyphase clock is inputted from the polyphase clock generation circuit so that a bit synchronizing operation is carried out at each different phase; and a selecting circuit for selecting outputs from the plurality of bit synchronous working circuits, based on the detection result of the detection circuit."

The same argument applies as well to the respective dependent claims. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

CONCLUSION

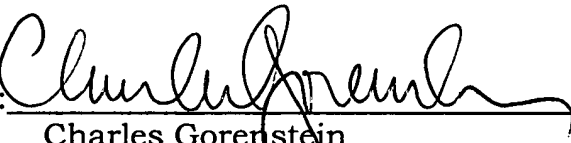
All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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